

TEJ100P/TEJ200P
TEJ100E/TEJ200E
TEJ101P/TEJ201P
TEJ101E/TEJ201E

Digital Trunk Interface Board

Hardware Manual

Version 1.0

Synway Information Engineering Co., Ltd www.synway.net



Contents

Conte	Contents				
Copyright Declaration Revision History					
1.1	Features	2			
1.2	Operation Principle	3			
Chap	oter 2 Installation	4			
2.1	Hardware Structure	4			
2.2	Interface Identification	9			
2.3	Slot Compatibility	9			
2.4	System Requirements	10			
2.5	Hardware Installation	10			
Appe	endix A Technical Specifications	13			
Appe	Appendix B Technical/Sales Support				



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Revision History

Version	Date	Comments
Version 1.0	2009-12	Initial publication.

Note: Only major revisions to this manual itself recorded herein.



Chapter 1 Overview

The Synway TEJ100P, TEJ200P, TEJ100E, TEJ200E, TEJ101P, TEJ201P, TEJ101E and TEJ201E are digital trunk interface boards which support E1, T1 and J1 environments. They are in 2U size, 120mm in length, compact in structure and high in integration. TEJ100P, TEJ200P, TEJ101P, TEJ201P include PCI bus while TEJ100E, TEJ200E, TEJ101E and TEJ201E include PCIe bus, designed especially for various application systems that require high performance.

They all perform echo cancellation by on-board DSPs. The enhanced capability of TEJ101P, TEJ101E, TEJ201P, TEJ201E in echo cancellation reaches 128ms for time delay estimation, which ensures high-quality voice talk without extra modules or devices to support echo cancellation. They are cost-effective. The design of on-board EMC and lightning-proof circuits further guarantee the security in use.

These boards are completely compatible with Asterisk at the hardware/driver level and support smooth connection to Asterisk platform. Therefore they have a lot of advanced call features.

Supported Data Modes: Cisco HDLC, HDLC, PPP, Multi-link PPP, Frame Relay. Supported Voice Modes:

- PRI CPE and PRI NET
 - NI1
 - NI2
 - EuroISDN
 - 4ESS(AT&T)
 - 5ESS(Lucent)
 - DMS100
- E&M
 - Wink
 - Feature Group B
 - Feature Group D
- FXO and FXS
 - Ground Start
 - Loop Start
 - Loop Start with Disconnect Detect

These boards connect Asterisk Server with PSTN, Channel Bank or PBX via T1, E1 or J1 interface to build a specialized telephony network environment. Figure 1-1 and Figure 1-2 below are typical application models with these boards.



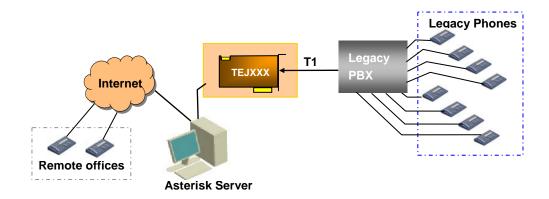
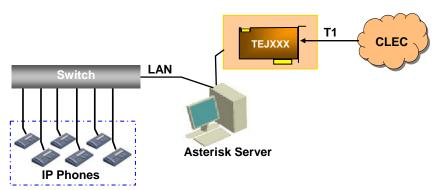


Figure 1-1 Application Model I: Traditional Telephony System



Note: TEJXXX in Figure 1-1 and Figure 1-2 represent available TEJ series boards
Figure 1-2 Application Model II: VoIP Telephony System

1.1 Features

PCI/PCIe Bus Support

TEJ100P/TEJ200P/TEJ101P/TEJ201P includes PCI 2.2 bus; in the universal PCI design, it supports 3.3V/5V PCI slot and PCI-X slot.

TEJ100E/TEJ200E/TEJ101E/TEJ201E includes PCle bus; supports PCl Express X1, X4, X8, X16 slots and PNP (plug and play) feature.

DMA Read and Write

The use of DMA technique for data reading and writing helps minimize the cost of the host CPU.

Compatible with Asterisk

Entirely compatible with Asterisk at the hardware/driver level, with all source codes open.

RJ48C Jack

The TEJ100P/TEJ100E/TEJ101P/TEJ101E and TEJ200P/TEJ200E/TEJ201P/TEJ201E boards respectively have 1 and 2 RJ48C jacks which can either connect directly with digital trunks or convert to BNC connectors via a proper adapter, making connection easy and malfunctions rare.



Echo Cancellation

The echo cancellers developed by Synway for these boards use on-board DSPs to work. TEJ101P/TEJ101E/TEJ201P/TEJ201E supports up to 128ms for time delay estimation per channel, and TEJ100P/TEJ100E/TEJ200P/TEJ200E supports 32ms, really cost-effective. It not only cancels out the effect of voice playback on DTMF and busy tones detection, but also avoids self-excited oscillation and howling, and minimizes the possibility of registering wrong DTMF and busy tones in a conference call, designed especially for VoIP application environments.

Voice CODEC Support

Supports A-law, µ-law codecs.

Clock Sync Support

Supports input and output of CT clock, allowing clock synchronization with multiple boards.

• EMC & Lightning-proof Circuits Available

1.2 Operation Principle

PCM Interface Outbound PCM Data Echo Inbound PCM Data Recording Playback Host Computer Interface (PCI/PCIe)

Figure 1-3 Operation Principle



Chapter 2 Installation

2.1 Hardware Structure

• TEJ100P, TEJ200P, TEJ101P and TEJ201P Boards

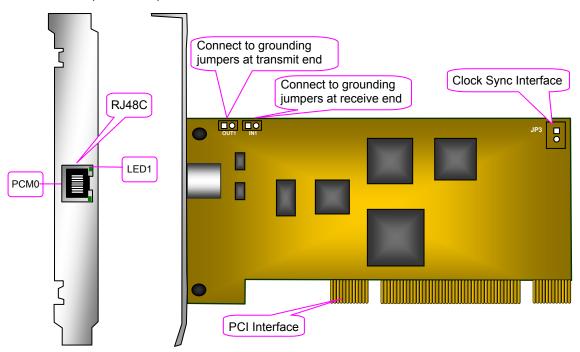


Figure 2-1 TEJ100P (Left and Front Views)

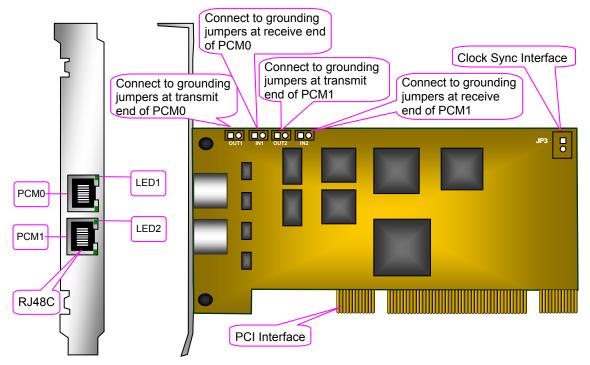


Figure 2-2 TEJ200P (Left and Front Views)



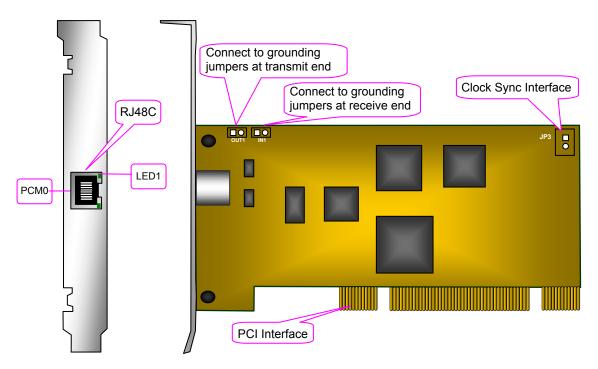


Figure 2-3 TEJ101P (Left and Front Views)

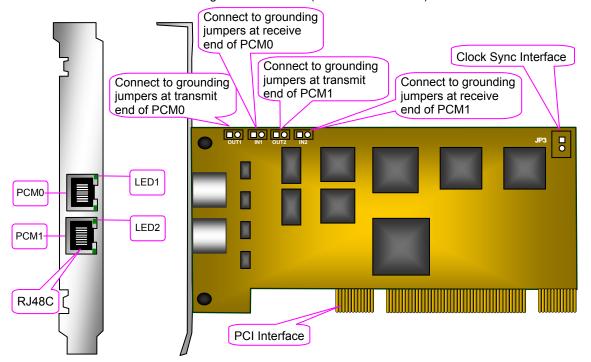


Figure 2-4 TEJ201P (Left and Front Views)



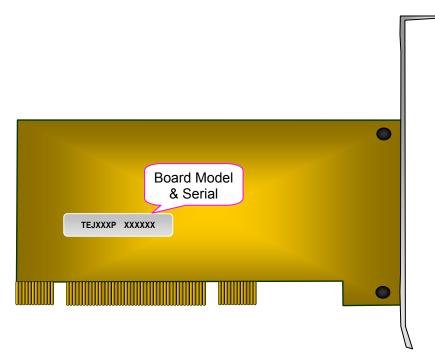


Figure 2-5 TEJ100P/TEJ200P/TEJ101P/TEJ201P (Rear View)

• TEJ100E, TEJ200E, TEJ101E and TEJ 201E Boards

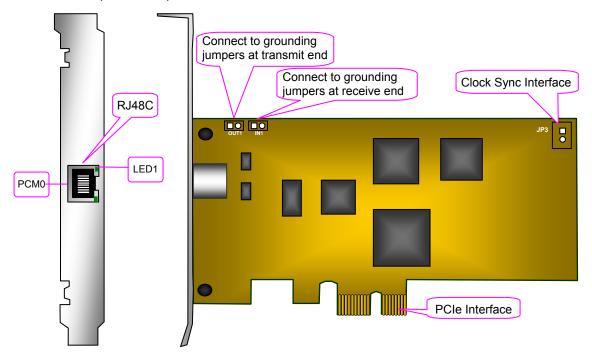


Figure 2-6 TEJ100E (Left and Front Views)



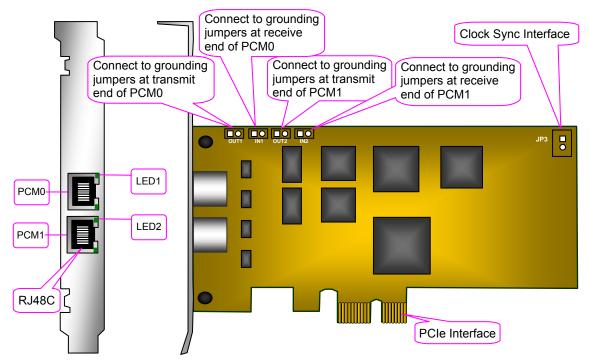


Figure 2-7 TEJ200E (Left and Front Views)

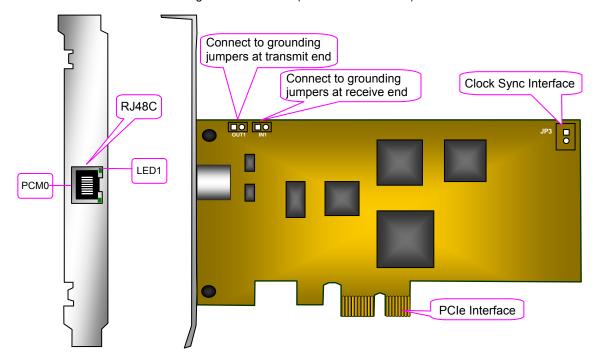


Figure 2-8 TEJ101E (Left and Front Views)



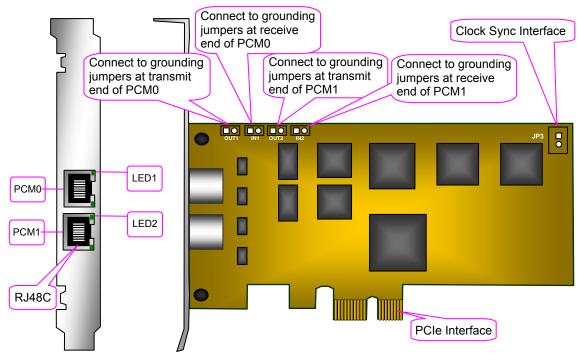


Figure 2-9 TEJ201E (Left and Front Views)

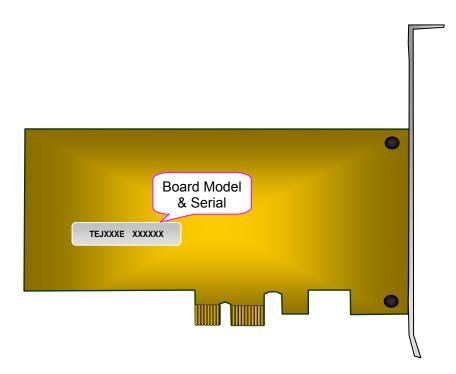


Figure 2-10 TEJ100E/TEJ200E/TEJ101E/TEJ201E (Rear View)

Notes:

- 1) PCM0~PCM1 in the above figures are 2 transmit/receive interfaces to trunks.
- 2) LED1 and LED2 are indicators for PCM0 and PCM1. They have three states as listed below.
 - ① On: PCM synchronous; ② Flashing: PCM not synchronous; ③ Off: Port unused



- 3) INm and OUTm respectively indicate the grounding jumpers at the receive and transmit ends, m=1~2. With regard to the configuration of grounding jumpers, refer to Step 1 in Section 2.5 Hardware Installation.
- 4) JP3 is an interface to the clock sync line.

2.2 Interface Identification

These boards all adopt 8-pin RJ48C jack. See Table 2-1 below for the pin layout of RJ48C.

	Pin	Note
	1	RRing
	2	RTip
Pin1	3	Not used
(4	4	TRing
Pin8	5	TTip
	6	Not used
	7	Not used
	8	Not used

Table 2-1 RJ48C

2.3 Slot Compatibility

Make sure it compatible with PCI or PCIe slots when using these boards. Users may choose whichever suitable according to the slot patterns illustrated in Figure 2-11 below.



Figure 2-11 PC Slots

Slot Number:

- 0: AGP Pro slot
- 1: 64-bit 5.0V PCI slot
- 2: 64-bit 3.3V PCI slot



- 3: 32-bit 5.0V PCI slot
- 4: PCI-Express x1slot
- 5: PCI-Express x8 slot
- 6: PCI-Express x4 slot
- 7: PCI-Express x16 slot

The TEJ100P, TEJ200P, TEJ101P and TEJ201P boards support the slots numbered 1, 2, 3 (i.e. PCI slots) in Figure 2-11; the TEJ100E, TEJ200E, TEJ101E and TEJ201E boards support the slots numbered 4, 5, 6, 7 (i.e. PCIe slots) in Figure 2-11 and the PNP (plug and play) feature.

2.4 System Requirements

Host System Requirements

CPU: 800MHz Intel® Pentium®III or above

Memory: 64M or more

HD: Depends on individual requirements

Supported Operating Systems

Linux: Debian, Fedora, Rad Hat

2.5 Hardware Installation

Note: Always turn off the power before installation!

Step 1: Configure the grounding jumper.

To use $100\Omega T1$, $110\Omega J1$ or $120\Omega E1$ balanced twisted-pair cable, disconnect all grounding jumpers.

In consideration of various line conditions, this series boards are equipped with two groups of grounding jumpers on each channel which respectively control the groundings of the transmitting and receiving ends. In case the $75\Omega E1$ unbalanced coaxial cable is used, the grounding jumpers at the receiving end should be disconnected while those at the transmitting end should be short-circuited, provided that the PC is properly grounded. This configuration is the factory default setting and applicable to most situations so that there is usually no need to change it. If it is difficult to ground the local PC, you may short-circuit the on-board grounding jumper at the receiving end and use the transmitting end at the opposite terminal for grounding. If the receiving end at the opposite terminal is grounded (improper operation), the on-board grounding jumper at the transmitting end must be disconnected. Refer to Table 2-2 for details.

Generally speaking, even in the case of proper grounding at both terminals, only the external layer of the E1 coaxial cable at the transmitting end is allowed to be grounded. The grounding of both transmitting and receiving ends may result in a current loop with ground wires, bringing instability to signals. Therefore, such grounding must be strictly avoided.



Opposite Terminal	Transmit End	grounded	grounded	non-grounded	non-grounded
Terminal	Receive End	non-grounded	grounded	non-grounded	grounded
PC grounded	Transmit End	short-circuited	disconnected	short-circuited	disconnected
PC grounded	Receive End	disconnected	disconnected	short-circuited	short-circuited
PC not	Transmit End	short-circuited	short-circuited	manage to make the PC grounded	short-circuited
grounded	Receive End	short-circuited	disconnected		short-circuited

Table 2-2 Configuration of Grounding Jumpers for Use of $75\Omega E1$ Unbalanced Coaxial Cable

Step 2: Properly fit the board onto the PC chassis.

It is suggested to fix the L-brackets on the board with screws before going to the next step.

Step 3: Connect to digital trunks.

Each board provides 1~2 RJ48C jacks, each of which can either connect directly with digital trunks or convert to 2 BNC connectors via an RJ48C-to-BNC adapter. See Figure 2-12 below.



Figure 2-12 RJ48C-to-BNC Adapter

Step 4: Set up an application environment.

Connect digital trunks with the on-board RJ48C jack to establish an application environment.

Step 5: Connect the clock sync line.

Note: Skip this step if there is no need of clock synchronization with multiple boards.

The on-board clock sync line is used to connect with other boards, such as digital trunk boards, analog boards from Synway or even boards from other companies, to offer a same clock to all boards connected together. This can reduce the error in faxing and guarantee the accuracy in data transmission between boards.



See Figure 2-13 below for the clock sync line provided by Synway.



Figure 2-13 Clock Sync Line

Step 6: Boot your computer and install the driver.

Regarding driver installation, refer to the file 'SynAST UserManual.doc' for details.



Appendix A Technical Specifications

Dimensions

120×64mm² (excluding L-bracket)

Weight

≤100g

Environment

Humidity: 10%—90% non-condensing

Storage humidity: 10%—90%

non-condensing

Input/output Interface

Digital trunk interface:

TEJ100P/TEJ100E/ TEJ101P/TEJ101E:

1 RJ48C jack

TEJ200P/TEJ200E /TEJ201P/TEJ201E:

2 RJ48C jacks

E1 interface:

Compliant with G.703, including 75 Ω unbalanced interface and 120 Ω balanced interface

T1/J1 interface:

DSX-1 and CSU line build-outs available for different extents of signal losses, including 100Ω and 110Ω balanced

interfaces

Audio Specifications

CODEC: CCITT A/µ-Law 64kbps

Distortion: ≤3%

Frequency response: 300-3400Hz (±3dB)

Signal-to-noise ratio: ≥38dB

Echo suppression: ≥40dB

Maximum System Capacity

Depends on the system consumption of Asterisk and the processing capability of

computer.

Power Requirements

+3.3V DC: 1000mA

Maximum power consumption: ≤5W

Audio Encoding & Decoding

A-Law 64kbps

μ-Law 64kbps

Sampling Rate

8kHz

Safety

Lightning resistance: Level 4



Appendix B Technical/Sales Support

Thank you for choosing Synway. Please contact us should you have any inquiry regarding our products. We shall do our best to help you. However, our technicians and salesmen are mainly responsible for maintaining our boards and providing relative technical support. If there are problems about Asterisk, please keep touch with Digium Inc. for help.

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